INTERFACING

Interfaceis the path for communication between two components. Interfacing is of two types, memory interfacing and I/O interfacing.

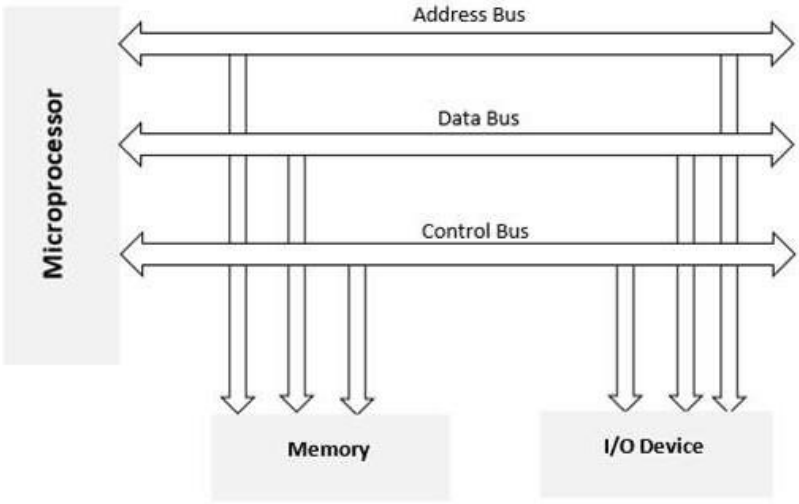
MemoryInterfacing

When we are executing any instruction, we need the microprocessor to access the memory for reading instruction codes and the data stored in the memory. For this, both the memory and the microprocessor requires some signals to read from and write to registers.The interfacing process includes some key factors to match with the memory requirements and microprocessor signals. The interfacing circuit therefore should be designed in such a way that it matches the memory signal requirements with the signals of the microprocessor.

IOInterfacing

There are various communication devices like the keyboard, mouse, printer, etc. So, weneed to interface the keyboard and other devices with the microprocessor by using latches and buffers. This type of interfacing is known as I/O interfacing.

BlockDiagramofMemoryandI/OInterfacing



8085InterfacingPins

Followingisthelistof8085pinsusedforinterfacingwithotherdevices−

- A_{15}-A_8(HigherAddressBus)

- AD_7-AD_0(LowerAddress/DataBus)
- ALE
- RD
- WR
- READY

WaysofCommunication–MicroprocessorwiththeOutsideWorld?

There are two ways of communication in which the microprocessor can connect with the outside world.

- SerialCommunicationInterface
- ParallelCommunicationinterface

Serial Communication Interface − In this type of communication, the interface gets a single byte of data from the microprocessor and sends it bit by bit to the other systemserially and vice-a-versa.

Parallel Communication Interface − In this type of communication, the interface gets a byte of data from the microprocessor and sends it bit by bit to the other systems in simultaneous (or) parallel fashion and vice-a-versa.

8257DMAController

DMAstands for Direct Memory Access. It is designed by Intelto transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU. Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

HowDMAOperationsarePerformed?

FollowingisthesequenceofoperationsperformedbyaDMA−

- Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMAcontroller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.

- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage theoperations over buses between the CPU, memory, and I/O devices.

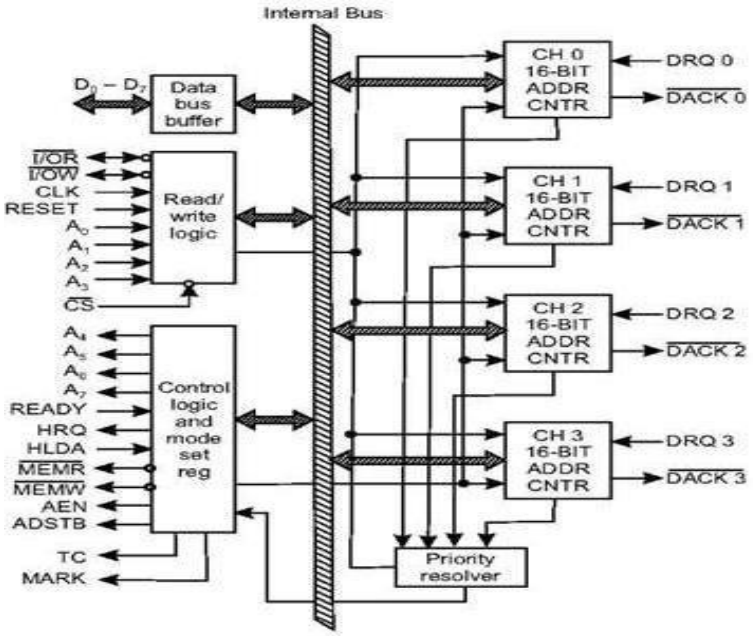
Featuresof8257

Hereisalistofsomeofthepro minentfeaturesof8257 −

- IthasfourchannelswhichcanbeusedoverfourI/O devices.
- Eachchannelhas16-bitaddressand14-bitcounter.
- Eachchannelcantransferdata upto64kb.
- Eachchannelcanbeprogrammedindependently.
- Eachchannelcanperformread transfer,writetransferand verifytransferoperations.
- It generates MARK signal to the peripheral device that 128 bytes have been transferred.
- Itrequiresasinglephase clock.
- Itsfrequencyrangesfrom250Hz to3MHz.
- Itoperatesin2modes,i.e.,**Mastermode**and**Slavemode**.

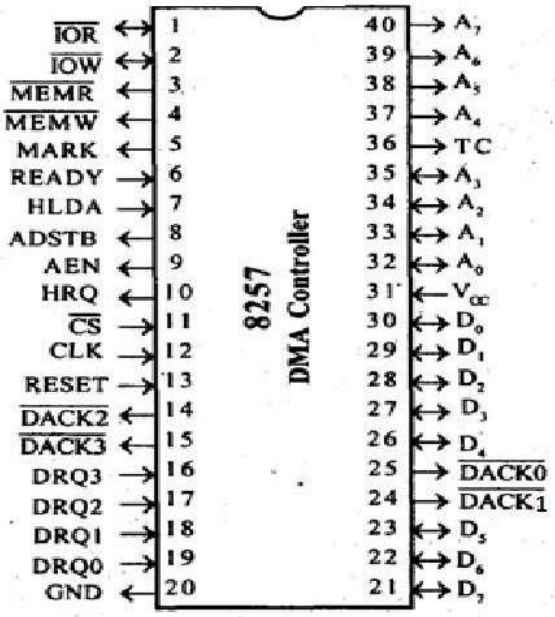
8257Architecture

The followingimageshowsthearchitectureof8257−



8257 PinDescription

Thefollowingimageshowsthepindiagramofa8257DMAcontroller −



DRQ$_0$−DRQ3 - These are the four-individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ$_0$ has the highest priorityand DRQ$_3$ has the lowest priorityamong them.

DACK$_0$− DACK$_3$- These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the statusoftheir request bythe CPU. These lines can also act as strobe lines for the requesting devices.

$D_0 - D_7$- These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the Slave mode, it carries command words to8257 and statusword from8257. Inthe master mode, these linesareused to send higher byte of the generated address to the latch. This address is further latched using ADSTB signal.

IOR - It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.

IOW - It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheraldevices during DMA memory read cycle.

CLK-Itisaclock frequencysignalwhich isrequired fortheinternaloperationof8257.

RESET - This signal is used to RESET the DMA controller by disabling all the DMA channels.

A_0 - A_3- These are the four least significant address lines. In the slave mode, they act as an input, whichselectsoneoftheregistersto beread orwritten. Inthemaster mode, theyarethe four least significant memory address output lines generated by 8257.

CS - It is an active-low chip select line. In the Slave mode, it enables the read/writeoperations to/from 8257. In the master mode, it disables the read/write operations to/from 8257.

A_4 - A_7- These are the higher nibble of the lower byte address generated by DMA in the master mode.

READY- Itisanactive-highasynchronous inputsignal, whichmakesDMAreadyby inserting wait states.

HRQ - This signal is used to receive the hold request signal fromthe output device. In the slave mode,it isconnectedwithaDRQ input line8257.InMastermode,it isconnectedwith HOLD input of the CPU.

HLDA-Itisthe holdacknowledgement signalwhichindicatestheDMAcontrollerthatthe bus has been granted to the requesting peripheral bythe CPU when it is set to 1.

MEMR-It isthe lowmemoryread signal, whichisused to readthedatafromtheaddressed memory locations during DMA read cycles.

MEMW-Itistheactive-lowthreestatesignalwhichisusedto writethedatatothe addressed memory location during DMA write operation.

ADST- Thissignalisusedto convertthehigherbyteofthe memoryaddressgeneratedby the DMA controller into the latches.

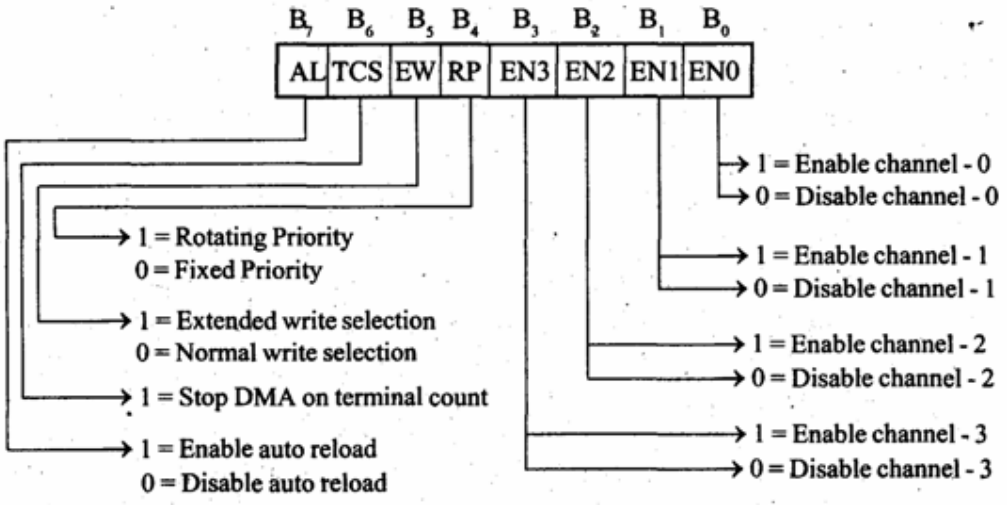
AEN-Thissignalisusedtodisabletheaddressbus/databus.

TC-Itstandsfor„TerminalCount“,whichindicatesthepresentDMAcycletothepresent peripheral devices.

MARK-The markwillbeactivatedaftereach128cyclesorintegralmultiplesofit fromthe beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

V_{cc}- Itisthepowersignalwhich isrequiredfortheoperationofthe circuit.

Controlwordformat



8255A-ProgrammablePeripheralInterface

The 8255A is a generalpurpose programmable I/O device designed to transfer the data from I/O to interrupt I/O under certain conditions as required. It can be used with almost any microprocessor.

It consists ofthree 8-bit bidirectional I/O ports (24I/O lines) which can be configured as per the requirement.

Portsof8255A

8255Ahasthreeports,i.e.,PORTA,PORTB,andPORTC.

- **PortA**containsone8-bitoutputlatch/bufferandone8-bitinputbuffer.
- **PortB**issimilar toPORTA.
- **Port C**can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word.

These three ports are further divided into two groups, i.e. Group A includes PORT A and upper PORT C. Group B includes PORT B and lower PORT C. These two groups can be programmed in three different modes, i.e. the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 2.

OperatingModes

8255Ahasthreedifferentoperatingmodes−

- **Mode 0** − In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports. Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched. Ports do not have interrupt capability.
- **Mode 1** − In this mode, Port A and B is used as 8-bit I/O ports. They can be configured as either input or output ports. Each port uses three lines from port C as handshake signals. Inputs and outputs are latched.
- **Mode 2**− Inthis mode, Port Acan be configured as the bidirectionalport and Port B either in Mode 0 or Mode 1. Port A uses five signals from Port C as handshake signals for data transfer. The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

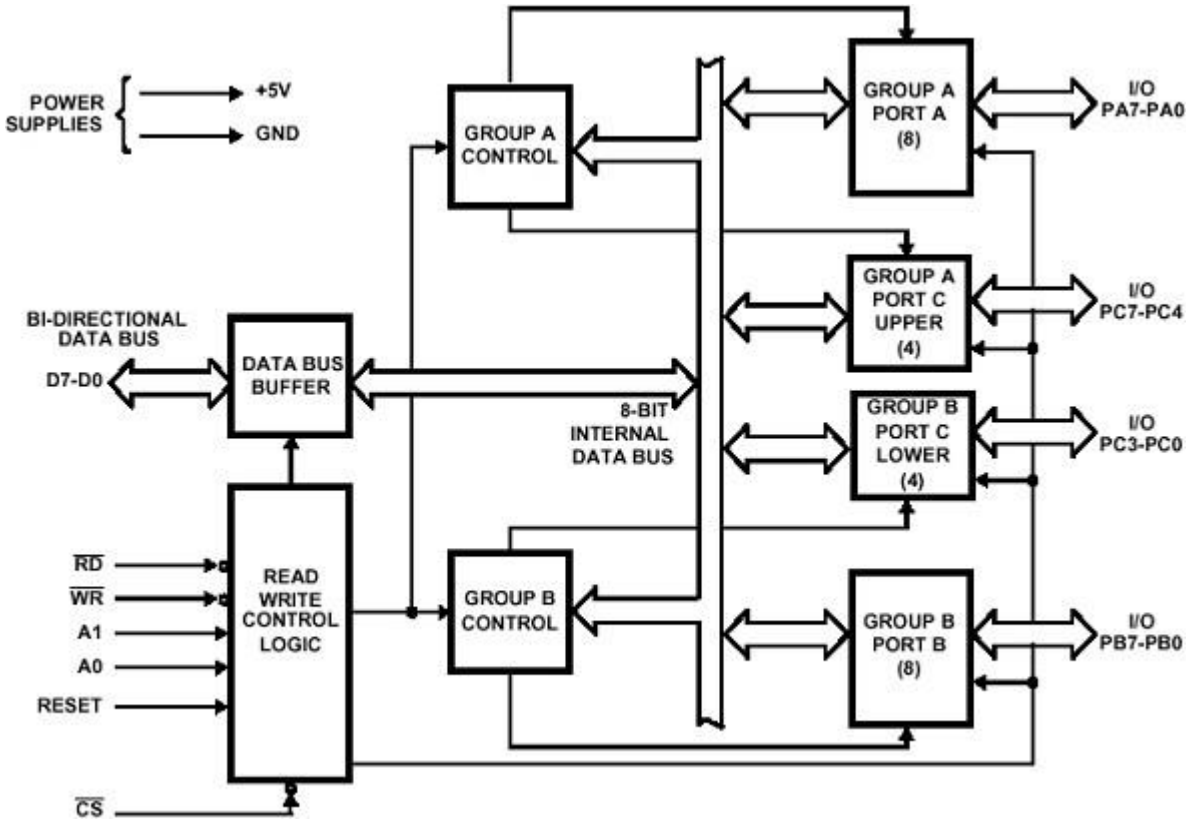
Featuresof8255A

Theprominentfeaturesof8255Aareas follows−

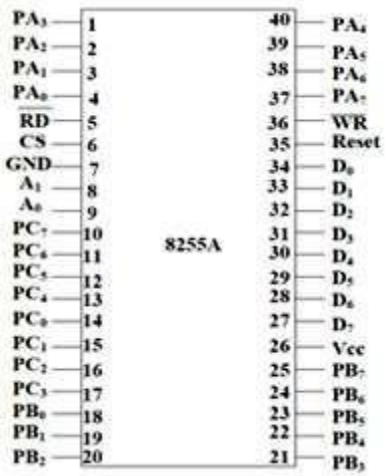
- Itconsistsof38-bitIOportsi.e.PA, PB,andPC.
- Address/databusmustbeexternallydemux'd.
- ItisTTLcompatible.
- IthasimprovedDCdriving capability.

8255Architecture

Thefollowingfigureshowsthearchitectureof8255A−



Letusfirstlookatthe pindiagramofIntel8255A−



Nowletusdiscussthefunctionaldescriptionofthepinsin8255A.

DataBusBuffer

It is a tri-state 8-bit buffer, which is used to interface the microprocessor to the system data bus. Data istransmittedor received bythe buffer asper the instructions bytheCPU. Control words and status information is also transferred using this bus.

Read/WriteControlLogic

This block is responsible for controlling the internal/external transfer of data/control/status word. It accepts the input from the CPU address and control buses, and in turn issues command to both the control groups.

CS

It stands for Chip Select. A LOW on this input selects the chip and enables the communication between the 8255A and the CPU. It is connected to the decoded address,and A_0& A_1 are connected to the microprocessor address lines.

Theirresultdependsonthefollowingconditions−

CS	A_1	A_0	Result
0	0	0	PORTA
0	0	1	PORTB

0	1	0	PORTC
0	1	1	ControlRegister
1	X	X	NoSelection

WR

Itstandsforwrite.Thiscontrol signalenablesthewriteoperation.Whenthissignalgoes low, the microprocessor writes into a selected I/O port or control register.

RESET

Thisisanactivehighsignal.Itclearsthecontrolregister and setsallportsintheinputmode.

RD

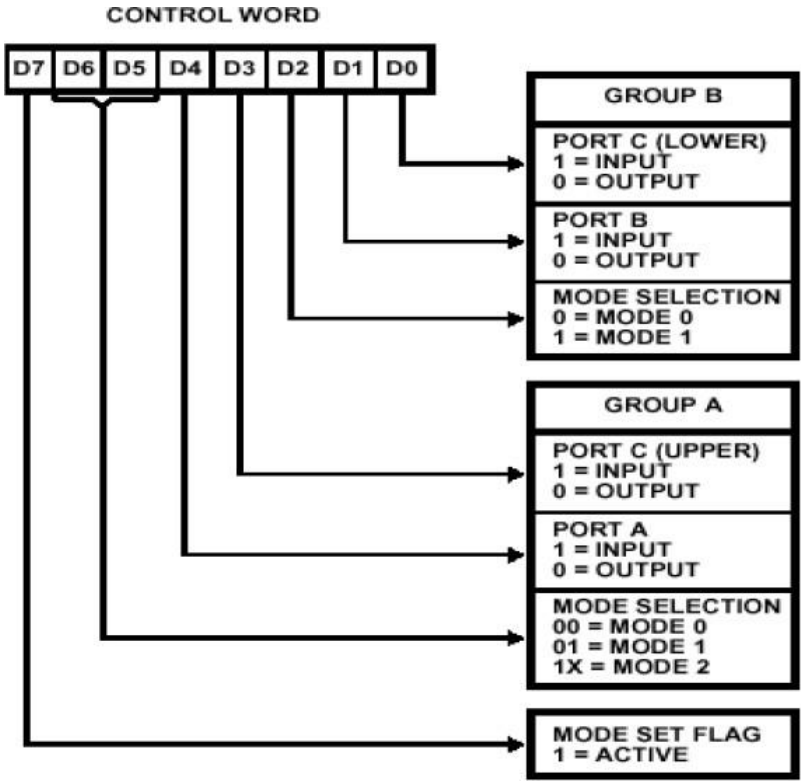
It stands for Read. This control signal enables the Read operation. When the signal is low,the microprocessor reads the data from the selected I/O port of the 8255.

A_0andA_1

These input signalswork withRD, WR, andone ofthe controlsignal. Following is thetable showing their various signals with their result.

A_1	A_0	RD	WR	CS	Result
0	0	0	1	0	**Input Operation** PORTA→DataBus
0	1	0	1	0	PORTB→Data Bus
1	0	0	1	0	PORTC→Data Bus
0	0	1	0	0	**OutputOperation** Data Bus→PORTA
0	1	1	0	0	Data Bus→PORTA
1	0	1	0	0	Data Bus→PORTB

1	1	1	0	0	Data Bus→PORTD



Intel8253/54-ProgrammableIntervalTimer

The Intel 8253 and 8254 are Programmable Interval Timers (PTIs) designed for microprocessors to performtiming and counting functions using three 16-bit registers. Each counter has 2 input pins, i.e. Clock & Gate, and 1 pin for "OUT" output. To operate a counter, a 16-bit count is loaded in its register. On command, it begins to decrement the count until it reaches 0, then it generates a pulse that can be used to interrupt the CPU.

Differencebetween8253and8254

Thefollowing tabledifferentiatesthefeaturesof8253 and 8254 −

8253	8254
Itsoperatingfrequencyis0-2.6MHz	Itsoperatingfrequencyis0-10MHz
It usesN-MOStechnology	It usesH-MOStechnology

Read-Backcommandisnot available	Read-Backcommandisavailable
Readsandwritesofthesamecountercannot be interleaved.	Readsandwritesofthesamecountercan be interleaved.

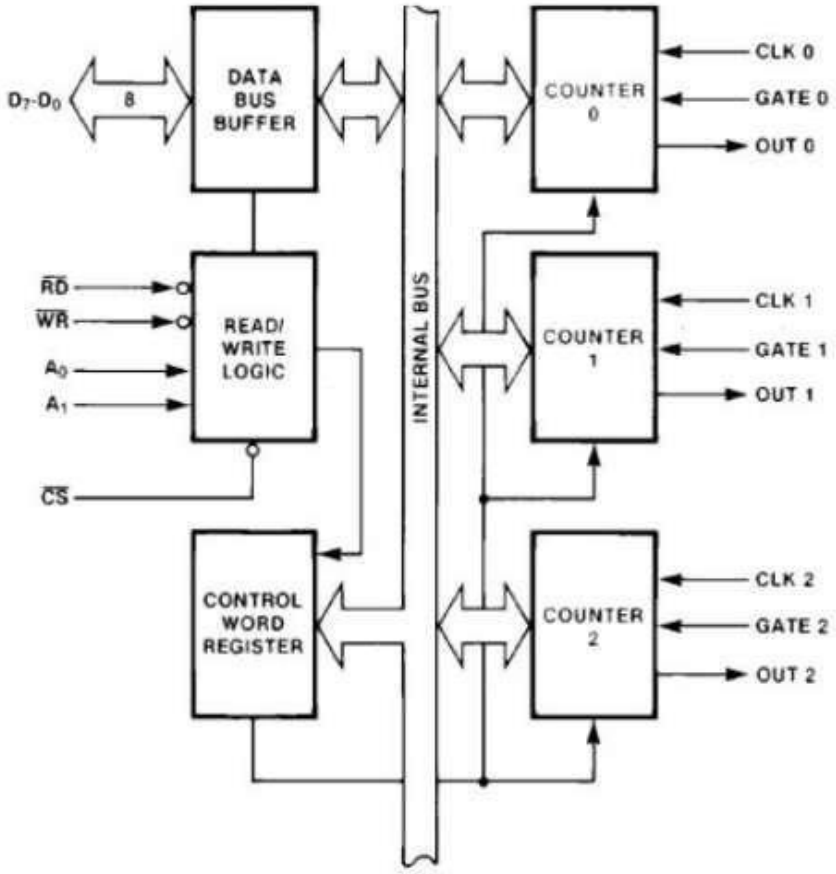
Featuresof8253/54

The mostprominentfeaturesof8253/54areasfollows−

- Ithasthreeindependent16-bitdowncounters.
- ItcanhandleinputsfromDCto10MHz.
- Thesethreecounterscanbeprogrammedfor either binaryor BCDcount.
- Itiscompatiblewithalmostallmicroprocessors.
- 8254 hasapowerfulcommand called READBACKcommand, whichallowstheuser to check the count value, the programmed mode, the current mode, and the status of the counter.

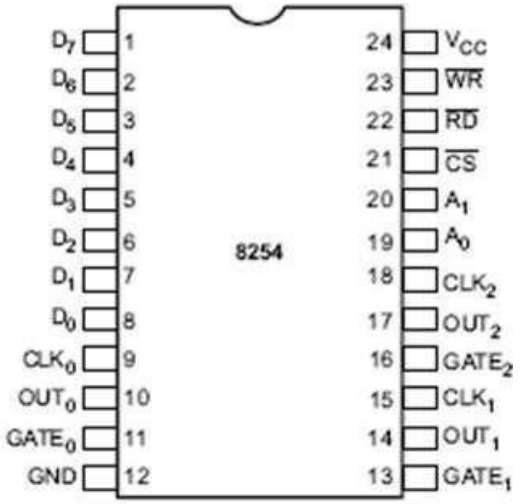
8254Architecture

Thearchitectureof8254 looksasfollows−



8254PinDescription

Hereisthe pindiagramof8254−



Inthe above figure, there are three counters, a databus buffer, Read/Write controllogic, and a control register. Each counter has two input signals - CLOCK & GATE, and one output signal - OUT.

Data Bus Buffer

It is a tristate, bi-directional, 8-bit buffer, which is used to interface the 8253/54 to the system data bus. It has three basic functions −

- Programmingthemodesof8253/54.
- Loadingthecount registers.
- Readingthecount values.

Read/WriteLogic

It includes 5 signals, i.e. RD, WR, CS, and the address lines A_0& A_1. In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively. In the memory mapped I/O mode, these are connected to MEMR and MEMW.

Address lines A_0& A_1 of the CPU are connected to lines A_0 and A_1 of the 8253/54, and CS istied to adecoded address. Thecontrolwordregister and countersareselected according to the signals on lines A_0& A_1.

A_1	A_0	Result
0	0	Counter0
0	1	Counter1
1	0	Counter2
1	1	ControlWordRegister
X	X	NoSelection

ControlWordRegister

This register is accessed when lines A_0& A_1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation. Following table shows the result for various control inputs.

A_1	A_0	RD	WR	CS	Result
0	0	1	0	0	WriteCounter0
0	1	1	0	0	WriteCounter1
1	0	1	0	0	WriteCounter2
1	1	1	0	0	WriteControl Word
0	0	0	1	0	ReadCounter0
0	1	0	1	0	Read Counter1
1	0	0	1	0	Read Counter2
1	1	0	1	0	Nooperation
X	X	1	1	0	Nooperation
X	X	X	X	1	Nooperation

Counters

Each counter consists of a single, 16 bit-down counter, which can be operated in either binary or BCD. Its input and output is configured by the selection of modes stored in the control word register. The programmer can read the contents of any of the three counters without disturbing the actual count in process.

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Intel8253/54-OperationalModes

8253/54canbeoperatedin6differentmodes.Inthischapter,wewilldiscussthese operational modes.

Mode0–InterruptonTerminalCount

- Itisusedtogenerateaninterrupttothemicroprocessorafter acertaininterval.
- Initially the output is low after the mode is set. The output remains LOW after the count value is loaded into the counter.
- The process of decrementing the counter continues till the terminal count is reached, i.e., the count become zero and the output goes HIGH and will remain high until it reloads a new count.
- The GATE signal is high for normal counting. When GATE goes low, counting is terminated and the current count is latched till the GATE goes high again.

Mode1–ProgrammableOneShot

- Itcanbeusedasamonostablemulti-vibrator.
- Thegateinputisusedasatriggerinputinthismode.

- Theoutputremains highuntilthecountisloadedandatriggerisapplied.

Mode2–RateGenerator

- Theoutput isnormallyhighafterinitialization.
- Whenever the count becomes zero, another low pulse is generated at the output andthe counter will be reloaded.

Mode3–SquareWaveGenerator

- Thismodeissimilar toMode 2 except the output remainslowfor half of the timer period and high for the other half of the period.

Mode4–SoftwareTriggeredMode

- Inthis mode, theoutput willremain highuntilthe timer has countedto zero, at which point the output will pulse low and then go high again.
- ThecountislatchedwhentheGATEsignalgoesLOW.
- Onthe terminalcount, the output goes low for one clock cycle thengoes HIGH. This low pulse can be used as a strobe.

Mode5–HardwareTriggeredMode

- Thismodegeneratesastrobeinresponsetoanexternallygenerated signal.
- This mode is similar to mode 4 except that the counting is initiated by a signalat the gate input, which means it is hardware triggered instead of software triggered.
- Afteritisinitialized,theoutputgoeshigh.
- Whentheterminalcountisreached, theoutputgoeslowforoneclockcycle.

INTEL8259AProgrammableInterruptController

The8259Aisaprogrammableinterruptcontrollerdesignedtoworkwith Intelmicroprocessor 8080 A, 8085, 8086, 8088. The 8259 A interrupt controller can

1) Handle eightinterrupt inputs. Thisis equivalent to providing eightinterrupt pins on the processor in place of one INTR/INT pin.

2) Vector an interrupt request anywherein thememory map.However,all the eightinterruptarespacedattheintervalofeitherfouroreightlocation.This

eliminates the majordrawback, 8085 interrupt, in which all interrupts are vectored to memory location on page 00H.

3) Resolveeightlevelsofinterruptpriorities inavarietyofmodes.

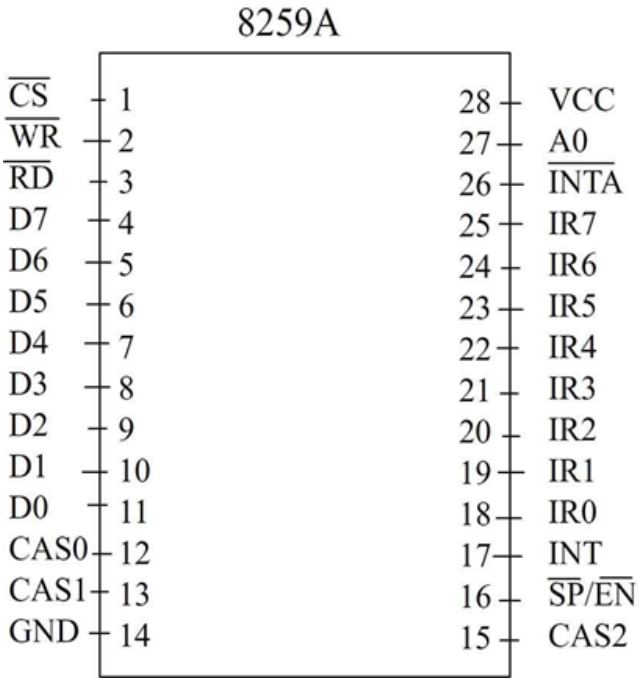
4) Maskeachinterruptrequestindividually.

5) Readthestatusofpendinginterrupts,inserviceinterrupts,andmasked interrupts.

6) Besetuptoaccepteitherthelevel triggeredoredgetriggeredinterruptrequest.

7) Mine8259ascanbecascadeinamasterslaveconfigurationtohandle64 interrupt inputs.

The 8259 A is contained in a 28-element in line package that requires only a compatible with 8259. The main difference between the two is that the 8259 A can be used with Intel 8086/8088 processor. It also induces additional features such as level triggered mode, buffered mode and automatic end of interrupt mode. The pin diagram and interval block diagram is shown below:



Thepinsaredefinedasfollows:

$\overline{CS}$ Chipselect -Toaccessthischip,is made low. ALOWonthispinenables $\overline{RD}$ & $\overline{WR}$ communication between the CPU and the 8259A. This pin is connected to address bus through the decoder logic circuits.

$\overline{WR}$ - A low on this pin. When $\overline{CS}$ is low enables the 8259 A to accept command words from CPU.

$\overline{RD}$ - A low on this pin whenis low enables these 8259 A to release status on to the data bus for the CPU. The status in dudes the contents of IMR, ISR or TRR register or a priority level.

D7-D0 - Bidirectional data bus control status and interrupt in a this bus. This bus is connected to BDB of 8085.

CAS0-CAS2 - Cascade lines: The CAS lines form a private 8259A bus to control a multiple 8259A structure ie to identify a particular slave device. These pins are outputs of a master 8259A and inputs for a slave 8259A.

$\overline{SP}$ /:$\overline{EN}$ Slaveprogram/enablebuffer:Thisis adual function pin.Itis usedas an input to determine whether the 8259A is to a master or as a slave.It is also usedasanoutput to disable thedatabus transceivers whendataare being transferred from the8259AtotheCPU. Wheninbuffered mode, it canbeusedasanoutput andwhen not in the buffered mode it is used as an input.

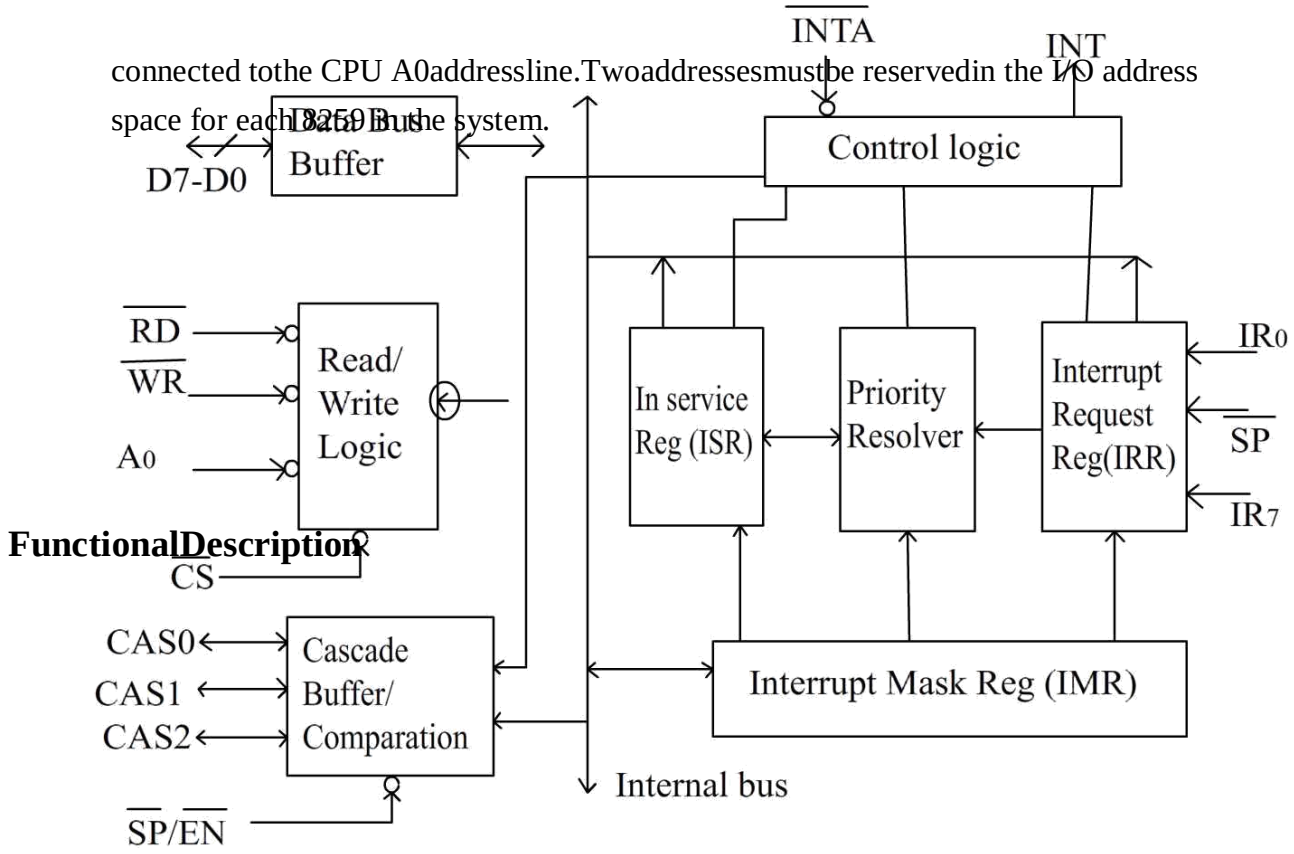
INT - This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU; thus, it is connected to the CPU‟s interrupt pin (INTR).

$\overline{INTA}$ -Interrupt:Acknowledge. Thispin isused to enable 8259A interrupt vector data onthe data bus bya sequence of interrupt request pulses issued bythe CPU.

IR0-IR7 - Interrupt Requests: Asynchronous interrupt inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged. (Edge triggered mode).or just by a high level on an IR input (levels triggered mode).

A0 - A0 address line: This pinacts inconjunctionwiththe,&pins. It is used by the 8259Atosendvariouscommandwordsfromthe CPU andtoreadthe status.Ifis

connected tothe CPU A0addressline.Twoaddressesmustbe reservedin the I/O address space for each8259 Bthe system.



FunctionalDescription

The8259Ahaseight interruptrequest inputs, TR2IR0.The8259 A usesits INToutput to interrupt the 8085A via INTR pin. The 8259A receives interrupt acknowledge pulses from the at itsinput. Vector address used by the 8085 A to transfer control to the service subroutine ofthe interrupting device, is provided by the 8259 A on the data bus. The 8259A isaprogrammabledevicethatmustbeinitializedbycommandwordssentbythe.After

initialization, the 8259 A mode of operation can be changed by operation command words from the. The descriptions of various blocks are,

Data bus buffer - This 3- state, bidirectional 8-bit buffer is used to interface the 8259A to the system data bus. Control words and status information are transferred through the data bus buffer.

Read/Write & control logic - The function of this block is to accept OUTPUT commands from the CPU. It contains the initialization command word (ICW) register and operation command word (OCW) register whichstorethe variouscontrolformats for device operation. This function block also allows the status of 8159A to be transferred to the data bus.

Interrupt request register (IRR) - IRR stores all the interrupt inputs that are requesting service. Basically, it keeps track of which interrupt inputs are asking for service. If an interrupt input is unmasked, and has an interrupt signal on it, then the corresponding bit inthe IRR will be set.

Interrupt mask register (IMR) -The IMR is used to disable (Mask) or enable (Unmask) individualinterrupt inputs. Eachbit inthis registercorrespondstothe interrupt input withthe same number. The IMR operation on the IRR. Masking of higher priority input will notaffectthe interruptrequest linesoflowerpriority. Tounmaskanyinterruptthecorresponding bit is set „0".

Inservice register(ISR) - The in-serviceregisterskeepstracksofwhich interrupt inputsare currentlybeingserviced.For eachinputthat iscurrentlybeingservicedthe corresponding bit will be set in the in-service register. Each of these 3-reg can be read as status reg.

Priority Resolver -This logic block determines the priorities of the set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

Cascade buffer/comparator - This function blocks stores and compare the IDS of all 8259A"s in the reg. The associated 3-I/O pins (CAS0-CAS2) are outputs when 8259A isused a master. Master and are inputs when8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the cas2-cas0. The slave thus selected will send its pre-programmed subroutine address on to the data bus during the next one or two successive $\overline{INTA}$ pulses.